REMARKS

Claims 1, 3-11, 22, 24, 25, and 30 are pending in the present application. Claim 22 was amended and claim 30 was newly presented in the after final amendment of December 2, 2005; the Examiner refused entry of those amendments finding them to require a new search. Those amendments are represented here for the purpose of entry with the present *Request for Continued Examination* whereby the Examiner may undertake said search.

Statement of the Substance of the Interview

Pursuant to 37 C.F.R. §1.133(b), Applicant requests that the following statement of the substance of the interview conducted on January 10, 2006 be made of record. In that telephone interview Examiner Jin Wang discussed claims 1, 4, 9, and 30 with Applicant's representative Robert Hayden.

With respect to independent claim 1, Applicant sought to verify which elements of Duluk et al. (US 6,664,959) the Examiner viewed as sequential logic circuits and to discuss the reasons why Applicant concludes that Duluk et al. does not teach a plurality of sequential logic circuits each configured with the functionality required by claim 1. In the *Final Office Action* mailed October 4, 2005 the Examiner equated Subrasterizer 9052, Column Selection 9054, and Sample Z Buffer 9055 with the sequential logic circuits of claim 1 (See *Final Office Action*, 12). In the interview, the Examiner for the first time additionally identified MCCAM array 9003 as a sequential logic circuit. No agreement was reached as to claim 1.

With respect to dependent claim 4, Applicant asserted that a reasonable interpretation of "edge function" in view of the Applicant's specification is a function of a normal vector, and Duluk et al. does not teach such a function. The Examiner asserted that the equations in columns 30 and 39 of Duluk et al. represent equations of a line and, although not expressed in terms of a normal vector, is in effect an edge function. No agreement was reached as to claim 4.

With respect to dependent claim 9, Applicant noted that the limitation that "the predetermined number of polygonal subportions is two" is not expressly taught by of Duluk et al. The Examiner referred to FIGs. 13A-C and column 39 (though in previous *Office Actions* the Examiner cited to columns 29-37). Applicant noted that in FIGs. 13A-C each stamp is divided into four pixels, not the required two. The Examiner asserted that modifying the stamps to include only two pixels instead of four would be an obvious modification. Applicant pointed out that if claim 9 were rejected under 35 U.S.C. § 103(a) the Examiner would have to provide a motivation for making the modification from four pixels per stamp to two. No agreement was reached as to claim 9.

With respect to independent claim 30, the Examiner noted that the claim was patentable over the existing references but insisted a new search was necessitated. Applicant asserted that a new search should not be required in view of the number of searches already performed over the course of the extended prosecution, and asked the Examiner to identify any claim limitation that would justify a further search. No agreement was reached regarding the necessity of a new search, though agreement was reached as to the patentability of claim 30 over the existing references of record.

Rejections of the Claims

Claims 28 and 29 are rejected under 35 U.S.C. § 102(e) as being anticipated by Greene et al. (US 6,480,205). Claims 1, 3, 4, 6, 7, 9, and 10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Duluk et al. in view of Bowen et al. (US 6,329,996). Claims 5 and 8 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Duluk et al. in view of Bowen et al. and Greene et al. (US 6,480,205). Claim 11 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Duluk et al. in view of Bowen et al. and Larson et al. (US 6,359,623). Claims 12-22, 24, 25 and 27 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Larson et al. in view of Greene et al.

Rejections Under 35 U.S.C. §102(e)

Claims 28 and 29 are rejected under 35 U.S.C. § 102(e) as being anticipated by Greene et al. The rejection of these two claims is moot in view of their cancellation.

Rejections Under 35 U.S.C. § 103(a)

Claim 1, 3, 4, 6, 7, 9, and 10

Claims 1, 3, 4, 6, 7, 9, and 10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Duluk et al. in view of Bowen et al. Claims 5 and 8 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Duluk et al. in view of Bowen et al. and Greene et al. Additionally, claim 11 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Duluk et al. in view of Bowen et al. and Larson et al.

The Applicant first notes that the Examiner, in the *Final Office Action*, did not specifically address the Applicant's arguments of August 1, 2005 regarding claim 1. See August 1 Response, 10-11. Instead, the Examiner repeated—verbatim—the arguments against patentability made in the previous rejection dated April 1, 2005. The Applicant respectfully reminds the Examiner that "[t]he applicant who is seeking to define his or her invention in claims that will give him or her the patent protection to which he or she is justly entitled should receive the cooperation of the examiner to that end" and "[t]he examiner should never lose sight of the fact that in every case the applicant is entitled to a full and fair hearing, and that a clear issue between applicant and examiner should be developed, if possible, before appeal." MPEP §706.07. Section 706.07 further provides that "the final rejection . . . should include a rebuttal of any arguments raised in the applicant's reply." MPEP §706.07.

The Applicant contends that simply declaring the arguments of the Applicant to be moot where the grounds of rejection are not new and absent countering the arguments previously submitted—as the Examiner has done in the present rejection—***does not rebut the arguments raised in Applicant's reply*** and does not further the goal of developing clear issues for appeal. The Applicant seeks the Examiner's cooperation and a full and fair hearing in order to define the claims. The Applicant further believes that

developing clear issues for appeal will be significantly hindered unless the Examiner directly addresses the Applicant's position on the previously cited prior art references.

The Applicant further notes that the Examiner, for the first time, has questioned whether claim 1 meets the written description requirement of 35 U.S.C. § 112, ¶ 1 but has not actually rejected any claims on this basis. See *Final Office Action*, 3. The Examiner has specifically questioned whether a logic circuit that receives two subtiles from a prior logic circuit, where the prior logic circuit subdivided a single tile to form the two subtiles, can be said to be receiving 'a different polygonal portion.' The Applicant asserts that the written description requirement is satisfied by the present disclosure.

The Applicant points out that each subtile in this example is different than the original tile. Thus, even though the subsequent logic circuit receives two subtiles that can be added to reconstruct the original tile, the subsequent logic circuit does receive 'a' different polygonal portion, as claimed. Here, as is accepted usage in claim construction, 'a' may mean 'one or more' as either of the subtiles represents a different polygonal portion.

The Applicant again returns to the points of distinction between the prior art references and claim 1. With respect to Duluk et al., the Applicant clearly demonstrated in the previous response that although Subrasterizer 9052 and Column Selection 9054 are logic circuits in series, the Column Selection 9054 ***does not*** determine the set of stamps within a stamp row that is touched by a primitive; only Subrasterizer 9052 performs this function. Claim 1, however, requires that '***each*** of the sequential logic circuits' is configured to 'determine whether the received polygonal portion is at least partly inside the graphics primitive.' Clearly, ***each*** of Subrasterizer 9052 and Column Selection 9054 ***does not*** determine the set of stamps within the stamp row that is touched by the primitive because Column Selection 9054 merely "tells the Z Cull unit 9012 which stamp to process in each clock cycle"; hence the name "Column Selection." Duluk et al. at col. 37, l. 10-12.

The Examiner has also equated Sample Z Buffer 9055 and MCCAM array 9003 as sequential logic circuits. "The Sample Z Buffer unit 9055 stores all the data for each sample in a tile, including the z value for each sample, and all the the [sic] sample FSM state bits." Duluk et al. at col. 37, l. 18-20. Accordingly, Sample Z Buffer 9055, as its

name implies, is merely a buffer and does not have the functionality of being able to 'determine whether the received polygonal portion is at least partly inside the graphics primitive' as required of ***each*** of the sequential logic circuits of claim 1.

Regarding MCCAM array 9003, Duluk et al. provides a detailed description of its operation with reference to FIG. 29:

> Cull block 9000 stores the z values for the opaque primitive samples in MCCAM array 9003 (shown in FIG. 15) (step 2901). The Sort block sends transparent primitives to the Cull block in the second and subsequent passes. In sorted transparency mode MCCAM array 9003 and Sample Z Buffer 9055 each store two z values (Zfar and Znear) for each corresponding sample. The Zfar value is the z value of the closest opaque sample. The Znear value is the z value of the sample nearest to, and less than, the z value of the opaque layer. One embodiment includes two MCCAM arrays 9003 and two Sample Z Buffers 9055 so as to store the Zfar and Znear values in separate units. First the z values for the front-most non-transparent samples are stored in the MCCAM array 9003 (step 2902). Duluk et al. at col. 48, l. 11-25.

It is clear that the MCCAM array 9003, like the Sample Z Buffer 9055, merely stores z values but does not 'determine whether the received polygonal portion is at least partly inside the graphics primitive' as required of ***each*** of the sequential logic circuits of claim 1.

The Applicant also wishes to point out that MCCAM Cull 9002 is not a logic circuit configured to 'determine whether the received polygonal portion is at least partly inside the graphics primitive.' "If MCCAM Cull 9002 cannot reject the primitive completely, it will generate a stamp list, each stamp in the list may contain a portion of the primitive that may be visible. This list of potentially visible stamps is sent to the Stamp Selection Logic 9008 of Cull block 9000. Stamp Selection Logic 9008 uses the geometry data of the primitive to determine the set of stamps within each stamp row of the tile that are actually touched by the primitive." Duluk et al. at col. 30, l. 2-9. Clearly, MCCAM Cull 9002 does not determine whether a polygonal portion is at least partly inside a graphics primitive. Rather, MCCAM Cull 9002 only determines a list of stamps that ***may*** contain a portion of the primitive. It is the Stamp Selection Logic 9008 that actually determines the stamps touched by the primitive.

Accordingly, the Applicant has shown that the only component of Cull block 9000 (FIG. 14) that can possibly be construed as a logic circuit configured to 'determine whether the received polygonal portion is at least partly inside the graphics primitive' is the Stamp Selection Logic 9008 and more particularly the Subrasterizer 9052 subcomponent of the Stamp Selection Logic 9008. As only a single subcomponent of the Cull block 9000 between the Input FIFO 9050 and the Sample State Machines 9057 (equated by the Examiner with the parallel logic circuits required by claim 1) can be considered to be a logic circuit configured to 'determine whether the received polygonal portion is at least partly inside the graphics primitive,' it follows that Duluk et al. does not teach a ***plurality*** of sequential logic circuits ***each*** configured to 'determine whether the received polygonal portion is at least partly inside the graphics primitive' as required by claim 1.

If the Examiner has identified any teaching in Duluk et al. that the Applicant has missed that supports a conclusion that any of the components distinguished above actually are configured to have the required functionality of the sequential logic circuits of claim 1, the Examiner is respectfully requested to particularly quote the portion of Duluk et al. relied upon, rather than merely citing to whole figures and columns. And as noted above, merely repeating that the Applicant's arguments are "moot" does not rebut these arguments and does not further the goal of developing clear issues for appeal.

The Applicant, in the previous response, also noted the further patentability of claims 4, 8, and 9. See August 1 Response, 11-12. The Examiner has not addressed these arguments. The Applicant respectfully requests that the Examiner review and address the arguments presented in the prior response regarding these claims. The Applicant also reminds the Examiner that in the interview of January 10 the rejection of claim 9 under 35 U.S.C. §102(e) was overcome.

Claims 12-22, 24, 25, and 27

Claims 12-22, 24, 25 and 27 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Larson et al. in view of Greene et al. The rejections of claims 12-21 and 27 are moot in view of their cancellation.

Claim 22, as amended, recites a method of identifying pixels inside a graphics primitive of a raster image comprising the step of recursively dividing into subtiles, over a number of cycles, each subtile larger than a pixel and having a portion within the graphics primitive and an other portion outside the graphics primitive. This step is further limited such that a maximum number of subtiles processed per cycle is a constant in each cycle of a first plurality of the number of cycles and increases for cycles of a second plurality of the number of cycles. The Applicant notes the support for the amendments to claim 22 can be found in the specification in at least paragraphs [0072] to [0081] and FIG. 11.

For example, sequential logic circuit 1102 receives a tile and subdivides it into two subtiles in one cycle. Sequential logic circuit 1104 then receives the two subtiles and subdivides those into as many as four subtiles in two cycles. Parallel logic circuit 1116 eventually receives as many as 256 tiles and subdivides them into as many as 512 subtiles in 8 cycles. In each successive logic circuit, the maximum number of subtiles per cycle is a constant—two—and the number of cycles required to handle the maximum number of subtiles increases by one. Parallel logic circuits 1118 and 1120, however, each receive as many as 256 tiles and subdivide them into as many as 512 subtiles as did parallel logic circuit 1116. Parallel logic circuits 1118 and 1120, however, receive and subdivide in parallel so that twice as many subtiles may be considered in the same number of cycles.

In the next 8 cycles, parallel logic circuits 1122 through 1128, together, consider as many as four times as many subtiles per cycle. Thus, the maximum number of subtiles processed per cycle increases to four during the cycles when parallel logic circuits 1118 and 1120 are processing and increase again to 8 during the cycles when parallel logic circuits 1122 through 1128 are processing. Thus, "[t]ogether, parallel logic circuits 1122 through 1128 can perform subdivision processing for as many as one-thousand-twenty-four (1024) subtiles in substantially one-eighth (1/8) the time it takes to process the subtiles sequentially." Specification, 24 at [0080].

Since neither Larson et al. nor Greene et al. teach or suggest the initial use of sequential processing followed by parallel processing to recursively divide a tile into subtiles, claim 22 and claims 24 and 25 depending there from are patentable over the

combination of Larson et al. and Greene et al. The Applicant therefore requests that the Examiner withdraw the rejection of claims 22, 24, and 25 under 35 U.S.C. §103(a).

New Claim 30

New claim 30 is supported by the specification by at least FIG. 11 and paragraphs [0072] to [0081]. None of the cited references—either alone or in combination—teach or suggest a graphics engine comprising a plurality of identical sequential logic circuits coupled in series followed by a plurality of identical parallel logic circuits where one parallel logic circuit provides polygonal subportions to two parallel logic circuits coupled in parallel. Accordingly, claim 30 is allowable over the cited art of record.

The Applicant particularly notes the patentability of claim 30 over Duluk et al. Claim 30 requires 'a sequential logic block comprising a plurality of identical sequential logic circuits coupled in series.' Although Stamp Selection Logic 9008 of Duluk et al. *may* be considered to be a sequential logic block, the Subrasterizer 9052 and the Column Selection 9054 thereof are not the claimed 'identical sequential logic circuits.'

Claim 30 also requires that a first sequential logic circuit of the plurality of sequential logic circuits is configured so that 'if the polygonal portion is at least partly inside the graphics primitive' the first sequential logic circuit will 'subdivide the polygonal portion into equal polygonal subportions and output the polygonal subportions.' The Subrasterizer 9052 of Duluk et al., however, "logically ORs the sixteen row masks to get the set of stamps touched by the primitive. Subraster 9052 then ANDs the touched stamps with the stamp selection bits 9278, as shown in tile 9276, to form one touched stamp list." Duluk et al. at col. 36, l. 41-45. The Subrasterizer 9052 combines a potential visible stamp list from MCCAM Cull "with the touched stamp list, to determine the final potentially visible stamp set in a stamp row," and "[f]or each row, the visible stamp set is sent to the Column Selection block 9054." Duluk et al. at col. 36, l. 46-52. The Subrasterizer 9052 of Duluk et al. ***does not*** subdivide a polygonal portion. Instead, when the Subrasterizer 9052 receives the stamp row, the stamp row is already divided into a set of stamps and the Subrasterizer 9052 is merely selecting amongst them.

Moreover, claim 30 requires that 'the last sequential logic circuit is configured to receive polygonal subportions, disregard any polygonal subportions thereof that are outside of the graphics primitive, and subdivide a remaining polygonal subportion into further equal polygonal subportions.' Even if Column Selection 9054 of Duluk et al. is considered to be an identical sequential logic circuit to Subrasterizer 9052, Column Selection 9054 does not 'subdivide a remaining polygonal subportion into further equal polygonal subportions' as is presently claimed. As noted above, Column Selection 9054 merely "tells the Z Cull unit 9012 which stamp to process in each clock cycle." Duluk et al. at col. 37, l. 10-12.

Further still, claim 30 requires 'a parallel logic block comprising a plurality of identical parallel logic circuits including a first parallel logic circuit configured to output still further subportions to two next parallel logic circuits operating in parallel.' There is no indication that Sample State Machines 9057 have a hierarchical structure where one Machine 9057 outputs data to two next Machines 9057 operating in parallel. Additionally, the claimed first parallel logic circuit is configured to 'disregard any further polygonal subportions that are outside of the graphics primitive, and subdivide a remaining further polygonal subportion into still further equal polygonal subportions.' There is no indication in Duluk et al., however, that the Sample State Machines 9057 have this functionality. Rather, "Sample State Machines 9057 [ ] each determine in parallel how to update the z value and sample state for the sample in the Z buffer it controls." Duluk et al. at col. 37, l. l. 42-44.

CONCLUSION

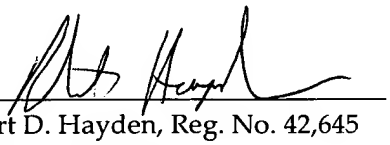
The Applicant respectfully requests the Examiner consider and comment as to the remarks pertaining to, at least, claim 1 submitted August 1, 2005. The Applicant contends, in light of the previously submitted and present remarks, claim 1 to be allowable over the cited references. All claims depending from claim 1 are, therefore, also allowable.

The Applicant contends claim 22 is allowable for at least the reasons set forth herein. All claims depending there from are also allowable.

The Applicant further contends claim 30 to be allowable in that the cited art of record fails to disclose the presently claimed system for identifying pixels inside a graphics primitive of a raster image.

The Applicant contends that all present rejections are overcome and, therefore, that all pending claims are allowable. The Applicant therefore respectfully requests a *Notice of Allowance*. Should the Examiner have any questions concerning the present amendment and arguments, the Applicant's undersigned attorney may be reached at the number set forth below.

Respectfully submitted,
Daniel H. McCabe

April 4, 2006 By: 

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